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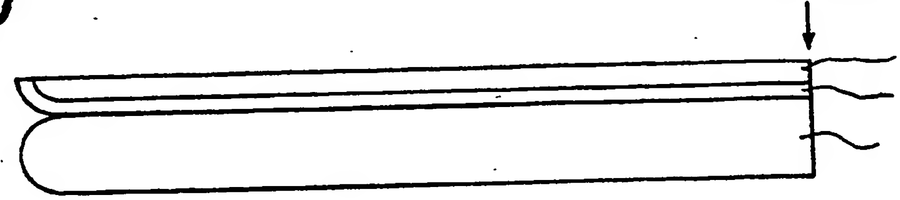
(54) **Method of manufacturing semiconductor substrate and method of manufacturing semiconductor device composed of the substrate.**

(57) Disclosed is a method of manufacturing a semiconductor wafer or SOI substrate having TTV of 1 micrometer or less which is required to make a future semiconductor integrated circuit of high density.

A semiconductor crystal disk (2; 12; 20, 21) made by slicing a semiconductor crystal ingot (1) is flattened by being subjected to a flattening step such as a grinding step (4), chemical-mechanical polishing or the like and then subjected to a step for providing an asymmetric configuration such as an orientation flat (OF) (12a, 21a) and the like. With this process, the deterioration of flatness due to the presence of the OF and the like can be prevented. Further, a flattening step conventionally carried out by a lapping step is replaced by surface grinding, by which the flatness of a wafer is improved and an etching step following to the lapping step can be omitted. The introduction of this process enables semiconductor wafers having a TTV of 1 micrometer or less and a diameter of 6 inches to be obtained at a yield of 90% or more. The application of the above method to an SOI substrate composed of two silicon wafers (20, 21) bonded through an insulating layer (22) can uniformly thin one of the silicon wafers to a few micrometers, whereby the practical use of a semiconductor integrated circuit of an SOI structure will be accelerated.

FIG. 10D



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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor substrate provided with a positioning means such as a so-called orientation flat (OF) or notch and to a semiconductor device made by using such a substrate.

Semiconductor devices tend to be more densely integrated, operated at a higher speed and made smaller in size at an increasing speed and accordingly the size of a pattern of elements constituting the semiconductor device is reduced, which requires a wafer to have a flat surface and a uniform thickness of 1 micrometer or less. Further, an approach using a substrate composed of two silicon wafers bonded through an insulating layer is most promising at present for providing a semiconductor device of high performance based on a so-called silicon on insulator structure (SOI) technology, in which one of the silicon wafers of the substrate must be thinned to a few micrometers.

Description of the Related Arts

A semiconductor wafer arranged as described above is usually made by the process shown in Figure 1, wherein (a) an ingot of a semiconductor single crystal having a desired composition is pulled up by a Czochralski method; (b) the ingot is roughly cut to a suitable length; (c) the side of the ingot is processed to have a cylindrical shape and further a plane parallel to the axis of the cylinder is formed on the side thereof, the plane serving as an OF to be described later; (d) the above ingot is sliced to many disks by a rotary blade type slicer; (e) the circumference thereof is beveled; (f) at least the surface thereof where a semiconductor device is to be formed is subjected to a lapping; (g) the disk is etched with a chemical solution; (h) mirror finished by a so-called chemical-mechanical polishing; and finally (i) cleaned to be finished. The mirror finished surface has flatness and crystallinity suitable to form a semiconductor device. The semiconductor wafer made by the above process is a disk having a straight cutout or the OF defined along a portion of the circumference thereof.

Although the etching at step (g) is carried out to remove crystal defects made on the wafer surface by the lapping at step (f), at this time the flatness of the disk is rather deteriorated by a different etching speed on the surface thereof caused by the nonuniform circulation of the etching solution and a temperature distribution thereof. However, the flatness is recovered by the polishing at step (h).

Nevertheless, the flatness of the semiconductor wafer made by the above process is limited to about 2 micrometers in terms of the value of a total thickness variation (TTV) which is a difference between the maximum value and the minimum value of the thickness of the wafer surface. Accordingly, the yield of wafers which satisfy the requirement of the flatness of 1 micrometer or less as described above is very low. This means that one of the bonded wafers is difficult to be uniformly thinned to a few micrometers or less in a process of making the above substrate having the SOI structure.

Summary of the Invention

An object of the present invention is to provide a practical method by which a semiconductor wafer having high flatness, specifically a TTV value of 1 micrometer or less can be fabricated at a good yield.

A further object of the present invention is to provide a method by which one of the wafers in a substrate having a SOI structure composed of two semiconductor substrates bonded through an insulating layer can be formed to a uniform thickness of a few micrometers or less.

To achieve these objects, first the present invention is characterized in that an asymmetric configuration such as an OF or notch provided to indicate the crystallographic direction of the semiconductor wafer is formed after the above flattening process has been carried out. Therefore, an asymmetric configuration such as the OF or the like is processed to one or both of the wafers in the above substrate having the SOI structure after the wafer on which a semiconductor device is to be formed has been subjected to a flattening process or mirror finish process. Second, the present invention is characterized in that a surface grinding is used in place of a conventional lapping and subsequent etching to flatten a disk made by slicing a semiconductor crystal ingot.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a chart explaining a conventional process for fabricating a semiconductor wafer;

Figure 2 is a chart explaining an embodiment of a process for fabricating a semiconductor wafer according to the present invention;

Fig. 3 (3A and 3B) is a schematic diagram explaining the principle of surface grinding;

Figure 4 is a graph explaining the improvement in the flatness of semiconductor wafers by using a surface grinding;

Fig. 5 (5A and 5B) is a graph explaining the deterioration of the flatness of semiconductor wafers by a chemical-mechanical polishing;

Fig. 6 (6A and 6B) is a graph showing the

change of the flatness of semiconductor wafers without an OF by a chemical-mechanical polishing;

Fig. 7 (7A and 7B) is a schematic perspective view showing an example of the deteriorated flatness of semiconductor wafers by the presence of an OF.

Fig. 8 (8A to 8D) is a schematic plan view explaining a mechanism for deteriorating the flatness of a semiconductor water by the presence of an OF;

Figure 9 is a schematic perspective view showing an example of a mark provided on the side surface of a semiconductor crystal ingot;

Fig. 10 (10A to 10E) is a schematic cross-sectional view explaining a process for fabricating an SOI substrate according to the present invention; and

Fig. 11 (11A to 11C) is a schematic cross-sectional view explaining a process for fabricating a semiconductor device composed of a semiconductor wafer according to the present invention.

PREFERRED EMBODIMENT

The inventors have obtained the following information from a preliminary study for improving the flatness of a semiconductor wafer:

i) when silicon wafers are subjected to a surface grinding using a grindstone in place of the lapping at step (f) of the above conventional process, good flatness can be obtained, and when a grindstone having a smaller grain size, a surface having less residual crystal distortion can be obtained as compared with that obtained by the lapping; and

ii) the triangular region defined by the OF and the lines connecting the center of a semiconductor wafer and the ends of the OF tends to be relatively thinner.

The above information implies that the time during which the etching is carried out at step (g) of the above conventional process may shortened or the etching itself may be omitted and further an amount of thickness thinned by the polishing at step (h) may be reduced by the employment of the surface grinding. It is also implied that an asymmetric configuration such as the OF may act to deteriorate the flatness of the a wafer surface in the process of flattening or mirror finishing the semiconductor wafer.

Therefore, the inventors have changed the process of fabricating a semiconductor water to the process shown in the chart of Figure 2, wherein the crystal pulling at step (a) to the cylindrical shaping of the ingot at step (c) are identical to those of Figure 1 except for the shaping of a plane to be used as an OF at step (c). The following sequence: (d) slicing the ingot to disks of semiconductor crystal; (e) beveling the circumference of the disk; (f) grinding the surface of the disk by a grindstone; (g) polishing the ground surface by a chemical-mechanical polishing; (h) providing the disk with an asymmetric configuration such as the OF; (i) beveling the OF portion; and finally, (j) cleaning the disk.

As described above, the process according to the present invention is mainly different from the above conventional process in that the surface grinding is carried out at step (f) of Figure 2 in place of the lapping at step (f) and the etching at step (g) of Figure 1 and that in Figure 2 the OF is formed after the surface grinding at step (f) and polishing at step (g) have been carried out.

According to the present invention, the surface of the sliced semiconductor crystal disk is ground using means such as a grindstone to a substantially predetermined thickness and flatness. Figure 3 is a schematic plan view (A) and side view (B) explaining the surface grinding, wherein a semiconductor crystal disk (wafer) 2 fixed on a stage 3 rotating clockwise is ground by a grindstone 4 rotating counterclockwise.

Figure 4 is a graph showing the improvement in the flatness realized by the above surface grinding as compared with the flatness of a semiconductor wafer subjected to the conventional lapping and etching, wherein the abscissa represents flatness in terms of TTV and the ordinate represents the ratio (%) of the number of semiconductor wafers, respectively. The above surface grinding was carried out using a high precision surface grinder from Sibayama Kikai KK (Osaka, Japan). The grindstone used was 150 cm in diameter and abrasive mesh about 8 micrometers. Figure 4 shows the result obtained from that silicon wafers having a diameter of 6 inches and a thickness of about 800 micrometers just after being sliced was surface ground by a thickness of 40 micrometers. Note that the specimens processed by the conventional process were silicon wafers having the same above dimensions and both sides thereof were lapped by a thickness of about 40 micrometers. The wafers of both groups were provided with on OF having a length of 55.5 mm.

As shown in the figure, the flatness of the lapped wafer surfaces distributes in the range of from 1.5 to 2.2 micrometers, whereas the flatness of the surface ground water distributes in the range of from 0.5 to 0.8 micrometer. More specifically, it is found that better flatness can be obtained by the surface grinding and the flatness is less dispersed among the respective wafers.

When the above surface ground wafers are subjected to the chemical-mechanical polishing at step (f) of Figure 2, however, the flatness thereof is

deteriorated, as shown in Figure 5. Figure 5A is a graph showing the distribution of flatness of the semiconductor wafers just after being surface ground and Figure 5B shows the distribution of flatness thereof after being surface ground and then polished, respectively, wherein the abscissa represents flatness in terms of TTV and the ordinate represents a ratio (%) of the number of semiconductor wafers, respectively. Note that Figures 5A and 5B show the result obtained from that 192 of silicon wafers each having a diameter of 6 inches and polished by 40 to 50 micrometers in thickness, respectively.

As shown in both figures, the TTV of the wafers just after being surface ground is within the range of from 0.4 to 0.8 micrometers and has an average value of 0.58 micrometers, whereas the TTV of the polished wafers distributes in the range of from 0.6 to 2.3 micrometers and has an average value of 1.21 micrometers. In the latter case, the number of the wafers having TTV of 1 micrometer or less is only 42% of the total number. However, the improvement achieved by the surface grinding is apparent in contrast with the fact that usual finished wafers have the distribution of TTV from 2.0 to 3.0 micrometers.

Above result suggests that when a semiconductor water is flattened or polished, asymmetry such as the OF may act to deteriorate flatness. Therefore, the inventor prepared silicon disks having a diameter of 6 inches and a thickness of 800 micrometers obtained by slicing an ingot without a plane formed on the side thereof for constituting OF, as described above. The disks are subjected to surface grinding, and hence to chemical-mechanical polishing. Figure 6 shows the flatness of these disks (wafers), wherein Figure 6A shows TTV distribution of 192 of the surface ground semiconductor wafers before the polishing and Figure 6B shows the TTV distribution of the these semiconductor wafers after being polished by 40 to 50 micrometers in thickness.

As shown in the figures, the TTV of the wafers before being polished distributes in the range of from 0.4 to 0.9 micrometer and has an average value of 0.61 micrometer, whereas the TTV of the wafers after being polished distributes in the range of from 0.5 to 1.3 micrometers and has an average value of 0.80 micrometers. However, 92% of the polished wafers have TTV of 1 micrometer or less. The flatness of the wafers surface ground without being provided with the OF is also deteriorated by the polishing, but it is apparent from the comparison of Figure 6B with Figure 5B that when the wafers not provided with the OF are surface ground, the deterioration of the flatness thereof caused by the polishing is greatly reduced.

Figure 7 is a schematic perspective view showing an example of the distribution of the measured heights of a wafer surface just after being surface ground, wherein Figure 7A shows a wafer not provided with the OF (although the wafer is not actually provided with the OF, the OF is illustrated for the convenience of a measuring instrument) and Figure 7B shows a wafer provided with an OF. The wafer surfaces have a TTV of 0.54 micrometers and 0.58 micrometers, respectively and no difference is admitted therebetween. In Figure 7A in which no OF is provided, however, any particular non-flatness is not shown on the surface, whereas in Figure 7B in which the OF is provided, the presence of recesses expanding from the center of the wafer toward the OF is apparently observed. Thus, it is found that although the effect of the OF does not eminently appear to the TTV, the OF affects the flatness.

The above relationship between the flatness of the wafer and the OF can be understood as follows. That is, it is assumed that the area of the a wafer 12 in contact with a surface grindstone 4 is different between the period during which an OF 12a overlaps the surface grindstone 4 as shown in Figures 8A to 8C and the period during which the OF 12a does not overlap the surface grindstone 4 as shown in Figure 8D. Accordingly, a non-uniform pressure is applied to the wafer 12, and the triangular region defined by the OF 12a and the lines connecting the center of the wafer 12 and the ends of the OF 12a tends to be relatively thinner. A similar problem also arises in the above chemical-mechanical polishing in which a polishing cloth and abrasive grains are pressed against a wafer surface.

As shown in Figure 6, when the OF is not provided, a given area of the wafer always comes into contact with the grindstone or a surface plate, and thus the uniformity in thickness is improved with the result that the TTV is made smaller. Note, at present the reason why the presnce of the OF less affects the surface ground wafer and greatly affects the polished wafer is not apparent.

From the above result, the surface flatness of most semiconductor wafers can be made to 1 micrometer or less in terms of TTV by the surface grinding. Further, the use of a less coarse surface grindstone can reduce the crystal distortion made on a wafer surface. Therefore, a subsequent chemical-mechanical polishing may be carried out in a minimum amount sufficient to remove the crystal distortion from the wafer surface. Further, the conventional lapping and etching using etchant can be substantially omitted.

Figure 2 shows a flow in which the OF is formed on the wafer after the surface grinding and subsequent polishing as described above. Since a surface having good flatness is formed by the

surface grinding, an amount of thickness lost in the subsequent polishing can be reduced. This means that even if the OF is formed following to the surface grinding and thereafter a polishing is carried out, the deterioration of the flatness can be sufficiently restricted to a low level. Alternately, a method may be employed by which a coarse polishing of about 10 micrometers in thickness is carried out prior to the formation of the OF and thereafter a final polishing of about 0.5 micrometer in thickness is carried out after the formation of the OF.

The OF is formed by a method as described below to the semiconductor wafer having been subjected to the above surface grinding or polishing. More specifically, an adhesive tape is applied to the back surface of the wafer, the wafer is fixed to the stage of a dicer through the adhesive tape by vacuum, and then the edge of the round wafer is entirely cut off at a speed of about 50 mm/min using the cutter of a dicer, similarly to a dicing process by which a wafer is cut off to chips. A cutting time per wafer is about 1 minute.

To ease the cutting for forming the above OF, a mark indicating a cutting position may be provided to the side of a semiconductor crystal ingot before it is sliced to disks. As shown in Figure 9, such a mark is a mark 11 composed, for example, of a straight shallow groove (marking-off) defined on the side of a cylindrically processed ingot 1 in parallel with the axis thereof. It is needless to say that the mark 1 is defined to be related to a crystallographic direction of the ingot 1. Further, the groove-shaped mark 11 is defined as shallow as possible so long as it does not disappear when the side of the semiconductor wafer is beveled later and does not remain in the effective surface area of the wafer after being beveled. Thus, the mark does not affect on the surface flatness in the processes of the above surface grinding and polishing. The groove may be formed by using a laser beam. The mark may be drawn with a waterproof ink. Further, when two marks each composed of the line of the above groove 11 or the like are provided on the side of the ingot 1, the OF can be easily formed in such a manner that the semiconductor wafer is cut off along the line connecting these two marks left on the edge of the semiconductor wafer.

A process of fabricating an SOI substrate composed of two bonded semiconductor wafers will be described with reference to Figure 10. Two wafers each having at least one surface chemically-mechanically polished in accordance with steps (a) - (g) of Figure 2 are prepared. Note that a mark indicating the crystallographic direction is formed on the side of each of these wafers in advance, as described above.

Next, as shown in Figure 10A, an oxide film 22 having a thickness of about 1 micrometer is formed to the surface of at least one of the above two wafers 20, 21 by, for example, a known thermal oxidization method. Then, these silicon wafers 20 and 21 are overlapped so that the above polished surfaces thereof confront to each other and subjected to a heat treatment in a nitrogen gas atmosphere at 1100°C. To increase a bonding force, a method of imposing a pulse voltage between the silicon wafers 20, 21 prior to the heat treatment is also known. Thus, the silicon wafers 20 is strongly bonded to the silicon wafer 21 through the oxidized film 22. Note that when the silicon wafers 20 and 21 are overlapped, the crystallographic directions thereof are related to each other on the basis of the above mark left on each side. Figure 10B is a plan view of the overlapped silicon wafers 20 and 21, wherein a circular flat surface and a beveled region therearound are shown.

Next, for example, the silicon wafer 21 is surface ground to a thickness of from 3 to 4 micrometers and further chemically-mechanically polished and thus is uniformly thinned to 2 micrometers, as shown in Figure 10C. Thereafter, as shown in Figure 10D and Figure 10E a corresponding plan view, the silicon wafers 20, 21 are cut on the basis of the above mark left on the side of the silicon wafer 20 to form an OF 21a. The mark on the side of the silicon wafer 21 may disappear at the steps wherein the oxide film 22 is formed and the wafer is thinned by being surface ground or polished as described above. Therefore, when the crystallographic directions of the silicon wafers 20 and 21 are related to each other at the step of overlapping them as described above, the crystallographic direction of the silicon wafer 21 can be found from the OF 21a. With this arrangement, an SOI substrate is completed which is composed of a silicon single crystal layer of 2 micrometers thick supported by a semiconductor wafer of several hundreds of micrometer thick through an insulating layer.

A semiconductor device is formed on the semiconductor wafer fabricated in accordance with the process shown in Figure 2 or on the SOI substrate fabricated in accordance with the process with reference to Figure 10. An embodiment thereof will be described with reference to the case in which the above SOI substrate is used. Figure 11A is a partially enlarged diagram of the SOI substrate shown in Figure 10D. An isolation region 25 is formed around a device region defined on the surface of the silicon wafer 21 made to the thickness of 2 micrometers in the substrate. The isolation region 25 may be any arbitrary structure such as a field oxide formed by a known local oxidation of silicon (LOCOS) method or a trench reaching the

oxide film 22.

Next, the surface of the silicon wafer 21 exposed at the each device region is thermally oxidized to form a gate insulating film 26 of about 200 angstroms thick, as shown in Figure 11B. Then, a gate electrode 27 composed, for example, of a polysilicon layer is formed using a known chemical vapor deposition (CVD) and lithography. Further, a resist mask 28 is formed on the surface of the SOI substrate to expose a predetermined device region and impurities such as arsenic (As) or the like are ion implanted to the silicon wafer 21 exposed from the resist mask 28 and gate electrode 27 to form a source/drain region 29.

Next, as shown in Figure 11C, an insulating layer 30 composed, for example, of phosphosilicate glass (PSG) is formed on the surface of the SOI substrate and a contact hole is formed at a predetermined position of the insulating layer 30. Thereafter, an aluminium layer is deposited on the insulating layer 30 and patterned by a known lithography to thereby form a gate wiring 31 and source/drain electrode 32 as shown in the figure, whereby a metal insulator semiconductor field effect transistor (MISFET) of a SOI structure is completed.

It is needless to say that the above OF 21a defined to the above SOI substrate is indispensable to align the mask with the SOI substrate at the above lithography step.

As described above, according to the method of fabricating a semiconductor wafer of the present invention, a surface having a large area can be more easily flattened as compared with a conventionally known method by which a polishing is carried out after dummy members having a thickness similar to that of a member to be processed having been disposed therearound. More specifically, in the above conventional method, the dummy members must have a thickness and material similar to those of the member to be processed and many man-hours are needed to spread the dummy members all around the member to be processed. Further, these dummy members cannot be reused. Therefore, the present invention is excellent in cost and mass-productivity.

As apparent from the above description, the method of manufacturing a semiconductor wafer according to the present invention is effective regardless of the size and material of the wafer. Further, it is needless to say that the SOI substrate according to the present invention is applicable not only to the manufacture of the MISFET as in the above embodiment but also to the manufacture of a bipolar transistor, a semiconductor device having a so-called Bi-MOS structure in which MISFETs and bipolar transistors are mixedly provided, and an integrated circuit composed of them.

Claims

1. A method of manufacturing a semiconductor substrate, comprising the steps of:
   forming an ingot (1) composed of semiconductor crystal and having a cylindrical side;
   slicing said ingot (1) to a disk (2; 12; 20, 21) having circular surfaces;
   applying a mechanical force to at least one of said circular surfaces to flatten the at least one circular surface; and
   providing a cutout (12a; 21a) to a portion of the circumference of said disk having said flattened circular surface so that said disk is rotationally unsymmetric with respect to a perpendicular having a foot at the center of said circular surface.

2. A method of manufacturing a semiconductor substrate according to claim 1, wherein said at least one circular surface is flattened with rotary grinding means (4).

3. A method of manufacturing a semiconductor substrate according to claim 1 or 2, wherein said cutout (12a; 21a) is provided by cutting off said disk (12; 20, 21) along a straight line connecting two points on the circumference of said disk.

4. A method of manufacturing a semiconductor substrate according to anyone of claims 1 to 3, further comprising the step of forming a straight mark (11) parallel to the rotationally symmetric axis of said ingot (1) on said side prior to slicing said ingot (1), so that said cutout (12a, 21a) is provided on the basis of said mark (11) left on the side of said disk (12; 20, 21) having said flattened circular surface.

5. A method of manufacturing a semiconductor substrate according to anyone of claims 1 to 3, further comprising the step of forming two straight marks (11) parallel to the rotationally symmetric axis of said ingot (1) on said side prior to slicing said ingot (1), so that said cutout (12a; 21a) is provided on the basis of said two marks (11) left on the side of said disk (12; 20, 21) having said flattened circular surface.

6. A method of manufacturing a semiconductor substrate according to claim 4 or 5, wherein said mark(s) (11) is formed by using a laser beam scanned on the side of said ingot (1).

7. A method of manufacturing a semiconductor substrate according to anyone of claims 1 to 6,

further comprising the step of beveling the side of said disk (20, 21) prior to the step of flattening said circular surface.

8. A method of manufacturing a semiconductor substrate according to anyone of claims 1 to 7, further comprising the step of mirror finishing said flattened circular surface.

9. A method of manufacturing a semiconductor substrate according to claim 8, wherein said mirror finishing is carried out by chemical-mechanical polishing.

10. A method of manufacturing a semiconductor device, comprising the steps of:
forming an ingot (1) composed of semiconductor crystal and having a cylindrical side;
slicing said ingot to a disk (21) having circular surfaces;
flattening at least one of said circular surfaces;
mirror finishing said at least one flattened circular surface; and
introducing impurities to a predefined region of the mirror finished surface of said disk (21).

11. A method of manufacturing a semiconductor substrate, comprising the steps of:
forming an ingot (1) composed of semiconductor crystal and having a cylindrical side;
slicing said ingot to a disk (20, 21) having circular surfaces;
flattening at least one of said circular surfaces;
mirror finishing said at least one flattened circular surface of each of said two disks (20, 21);
forming an insulating layer (22) on said mirror finished surface of at least one (20) of said two disks (20, 21); and
bonding said mirror finished surfaces of said two disks (20, 21) with the intervention of said insulating layer (22) therebetween.

12. A method of manufacturing a semiconductor substrate according to claim 11, wherein said two disks (20, 21) are aligned each other on the basis of a predetermined crystallographic orientation.

13. A method of manufacturing a semiconductor substrate according to claim 12, further comprising the steps of:
forming at least one straight mark (11) parallel to the rotationally symmetric axis of said ingot (1) on said side prior to slicing said ingot (1); and
aligning said two disks (20, 21) on the basis of said marks (11) left on the sides of said disks (20, 21) so that the disks (20, 21) of said substrate have said predetermined crystallographic orientation.

14. A method of manufacturing a semiconductor substrate according to anyone of claims 11 to 13, further comprising the step of beveling the side of said disk (20, 21) prior to the step of flattening at least one of said circular surfaces.

15. A method of manufacturing a semiconductor substrate according to anyone of claims 11 to 14, wherein said at least one circular surface of each of said two disks (20, 21) is flattened with rotary grinding means (4).

16. A method of manufacturing a semiconductor substrate according to anyone of claims 11 to 15, wherein said mirror finishing is carried out by chemical-mechanical polishing.

17. A method of manufacturing a semiconductor substrate according to anyone of claims 11 to 16, further comprising the step of thinning (21) one of said two disks (20, 21) after the step of bonding said mirror finished surfaces.

18. A method of manufacturing a semiconductor substrate according to claim 17, wherein the step of thinning said one disk (21) is performed with rotary grinding means (4).

19. A method of manufacturing a semiconductor substrate according to claim 17 or 18, further comprising the step of mirror finishing the surface of said thinned disk (21).

20. A method of manufacturing a semiconductor substrate according to claim 19, wherein the step of mirror finishing the surface of said thinned disk (21) is carried out by chemical-mechanical polishing.

21. A method of manufacturing a semiconductor substrate according to anyone of claims 17 to 20, further comprising the step of providing a cutout (21a) to a portion on the circumference of the counterpart disk (20) of said thinned disk (21).

22. A method of manufacturing a semiconductor substrate according to claim 21, wherein said cutout (21a) is provided by cutting off said counterpart disk (20) along a straight line connecting two points on the circumference of

said counterpart disk (20).

23. A method of manufacturing a semiconductor device, comprising the steps of:
forming an ingot (1) composed of semiconductor crystal and having a cylindrical side;
slicing said ingot (1) to a disk (20, 21) having circular surfaces;
flattening at least one of said circular surfaces;
mirror finishing said at least one flattened circular surface of each of said two disks (20, 21);
forming an insulating layer (22) on said mirror finished surface of at least one (21) of said two disk (20, 21)
bonding said mirror finished surfaces of said two disks (20, 21) with the intervention of said insulating layer (22) therebetween;
thinning one (21) of said two disks (20, 21) after the step of bonding said mirror finished surfaces;
mirror finishing the surface of said thinned disk (21);
introducing impurities to a predefined region (25, 29) of the mirror finished surface of said thinned disk (21).

24. A method of manufacturing a semiconductor device, comprising the steps of:
forming an ingot (1) composed of semiconductor crystal and having a cylindrical side;
slicing said ingot (1) to a disk (20, 21) having circular surfaces;
- flattening at least one of said circular surfaces;
mirror finishing said at least one flattened circular surface of each of said two disks (20, 21);
forming an insulating layer (22) on said mirror finished surface of at least one (21) of said two disks (20, 21)
bonding said mirror finished surfaces of said two disks (20, 21) with the intervention of said insulating layer (22) therebetween;
thinning one (21) of said two disks (20, 21) after the step of bonding said mirror finished surfaces;
providing a common cutout (11) to a portion of the circumference of each of said two disks (20, 21) after the step of thinning one (21) of said two disks (20, 21);
providing a common cutout (21a) to a portion of the circumference of each of said two disks (20, 21) after the step of thinning one of said two disks (20, 21) so that said two disks (20, 21) are rotationally unsymmetric with respect to a perpendicular having a foot at the center of the surface of said thinned disk (21);
mirror finishing the surface of said thinned disk (21); and
introducing impurities to a predefined region (25, 29) of the mirror finished surface of said thinned disk (21) aligned on the basis of said cutout (11, 21a).

FIG. 1 PRIOR ART

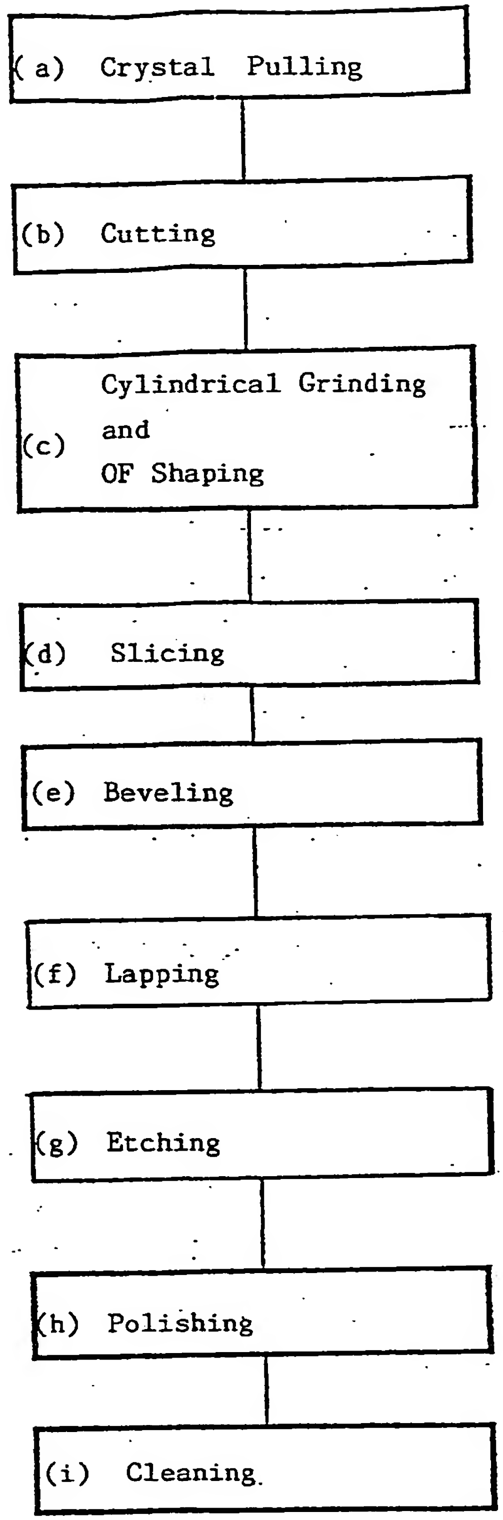


FIG. 2

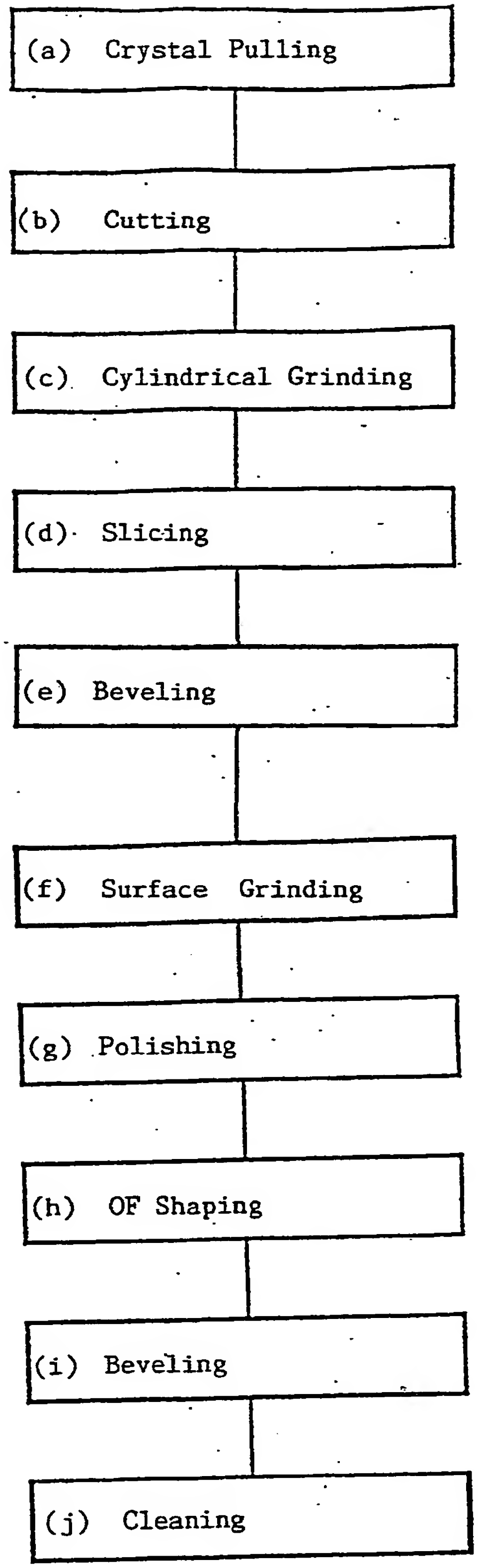

(a) Crystal Pulling
(b) Cutting
(c) Cylindrical Grinding
(d) Slicing
(e) Beveling
(f) Surface Grinding
(g) Polishing
(h) OF Shaping
(i) Beveling
(j) Cleaning

FIG. 3A

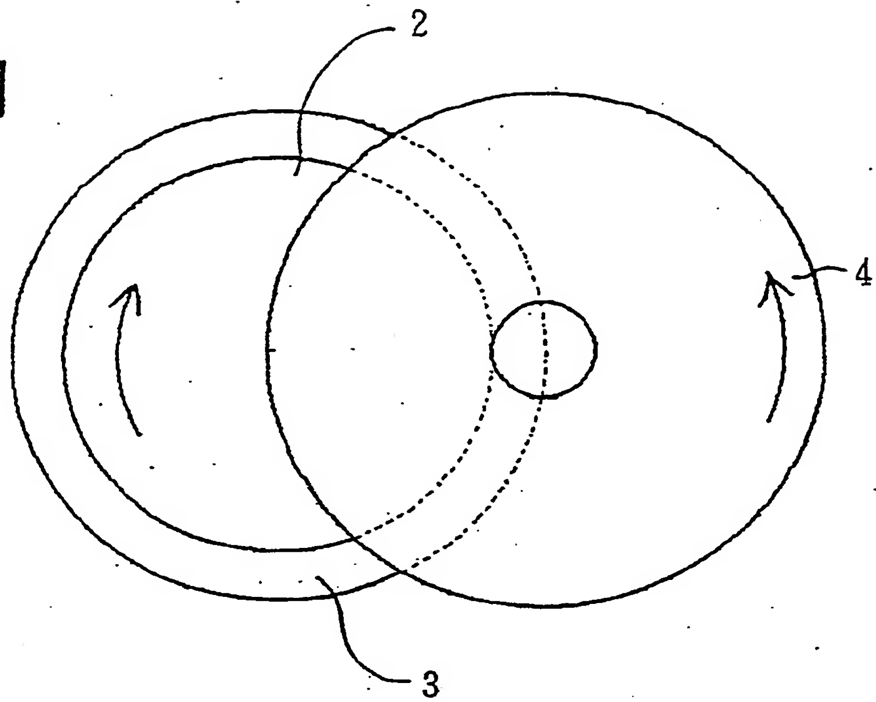


FIG. 3B

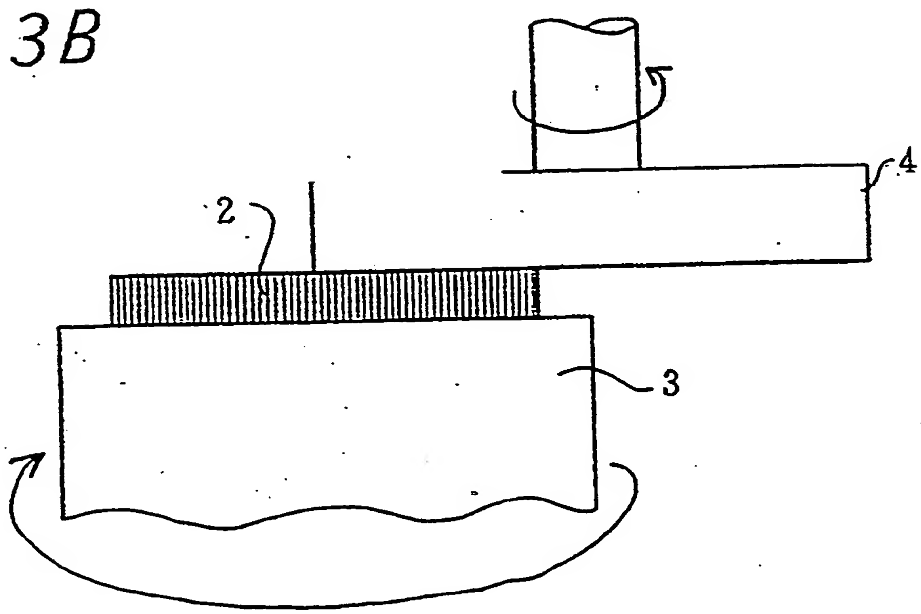


FIG.4

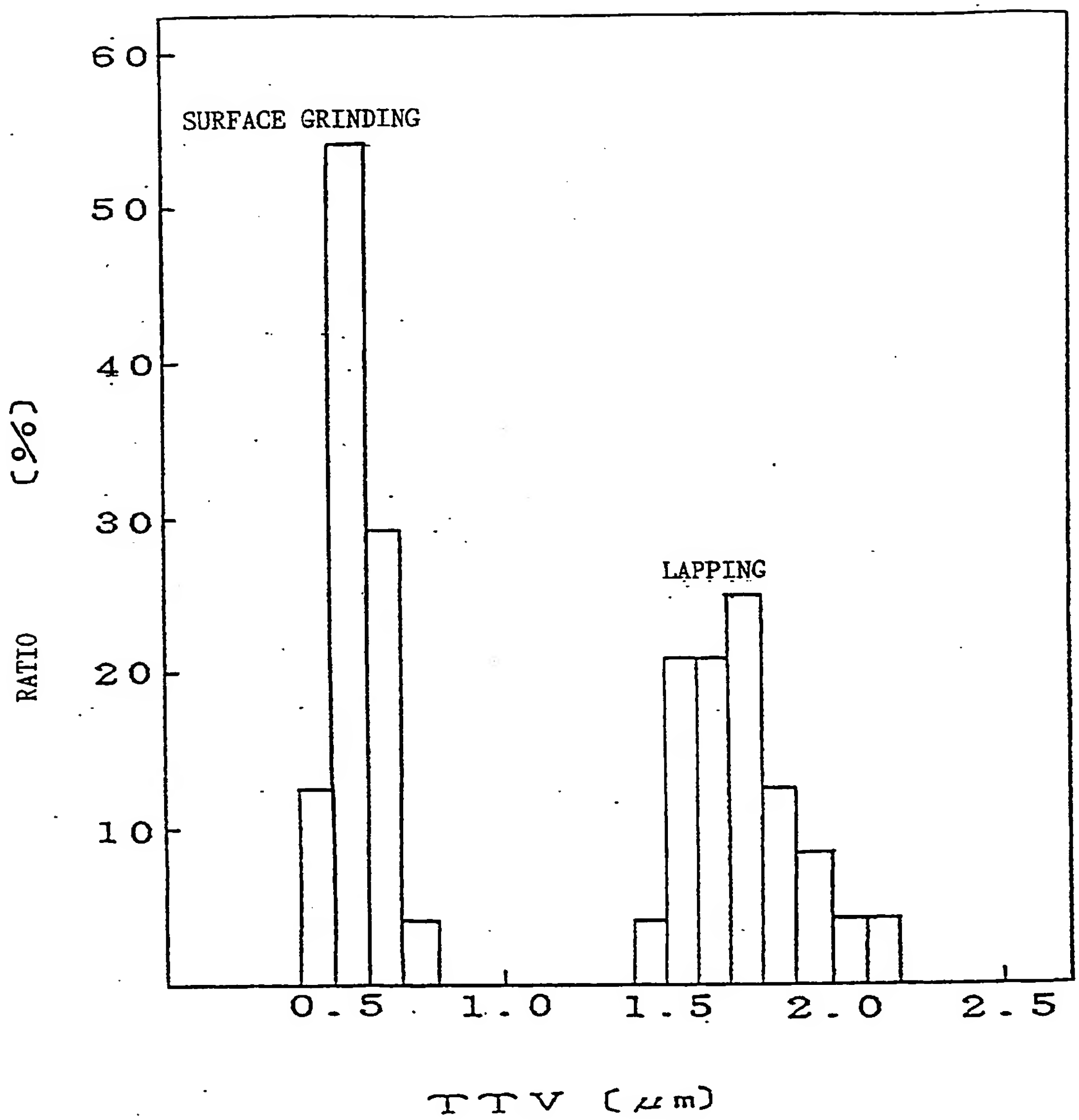

60
50
40
30
20
10
SURFACE GRINDING
LAPPING
RATIO (%)
0.5
1.0
1.5
2.0
2.5
TTV (μm)

FIG. 5 A

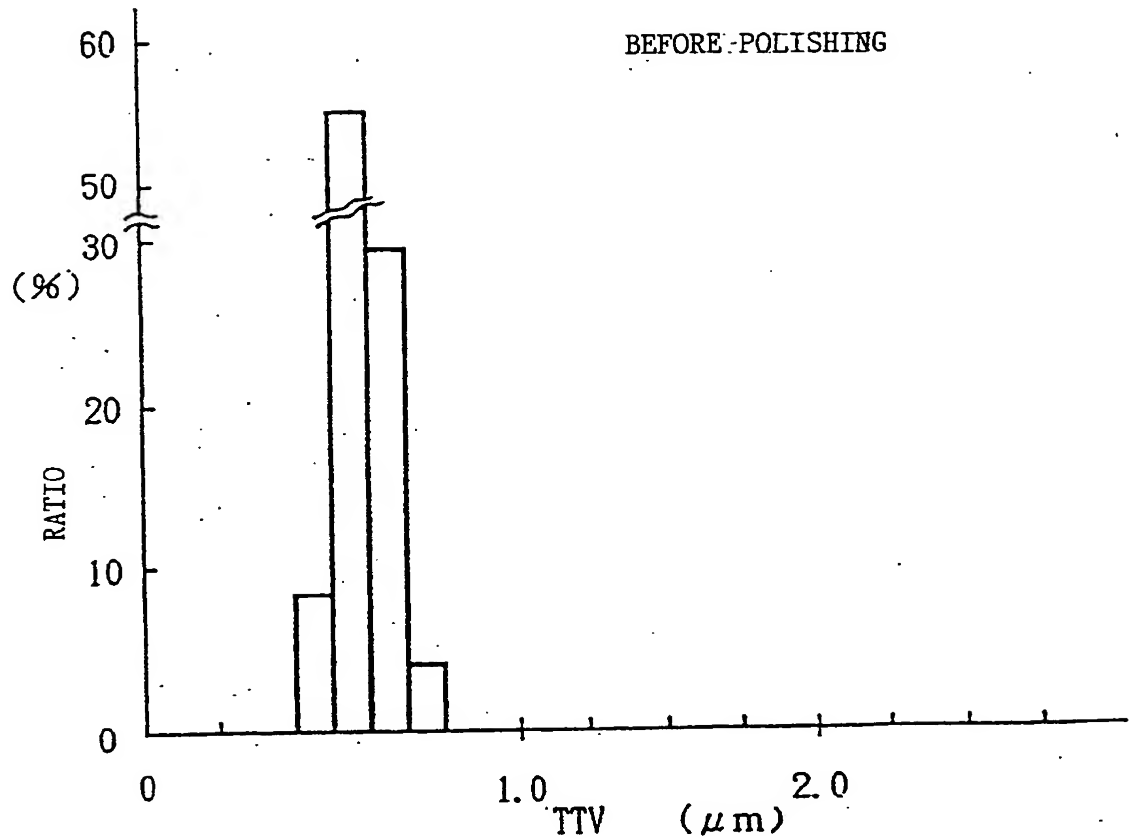

BEFORE POLISHING
60
50
30
(%)
RATIO
20
10
0
0
1.0
2.0
TTV (μm)

FIG. 5 B

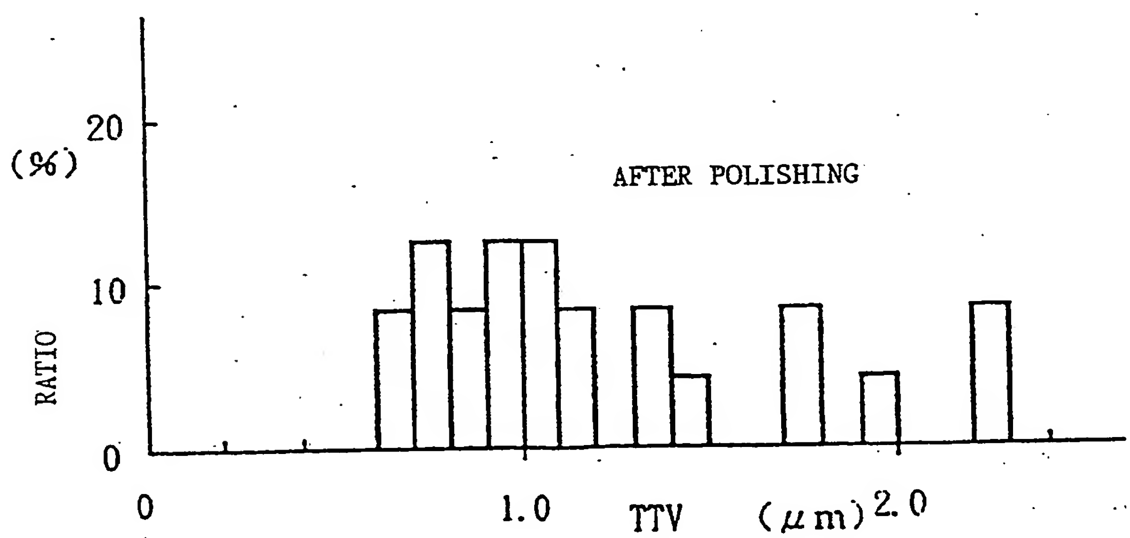

20
(%)
AFTER POLISHING
10
RATIO
0
0
1.0
TTV (μm)
2.0

FIG. 6A

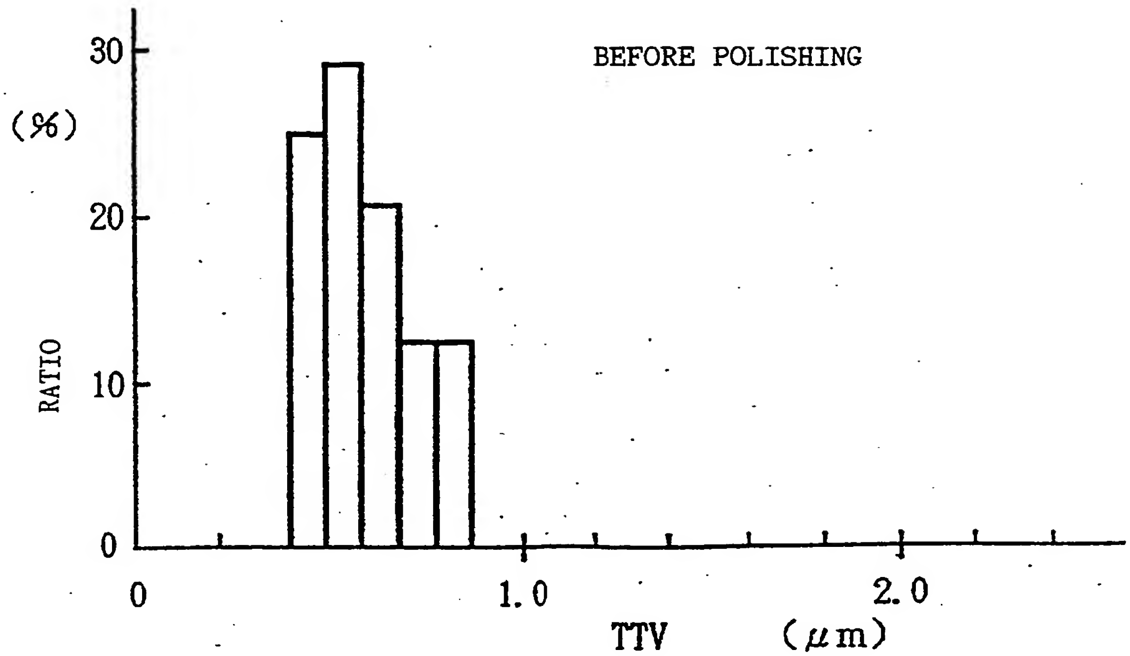

BEFORE POLISHING
30
(%)
20
RATIO
10
0
0
1.0
2.0
TTV (μm)

FIG. 6B

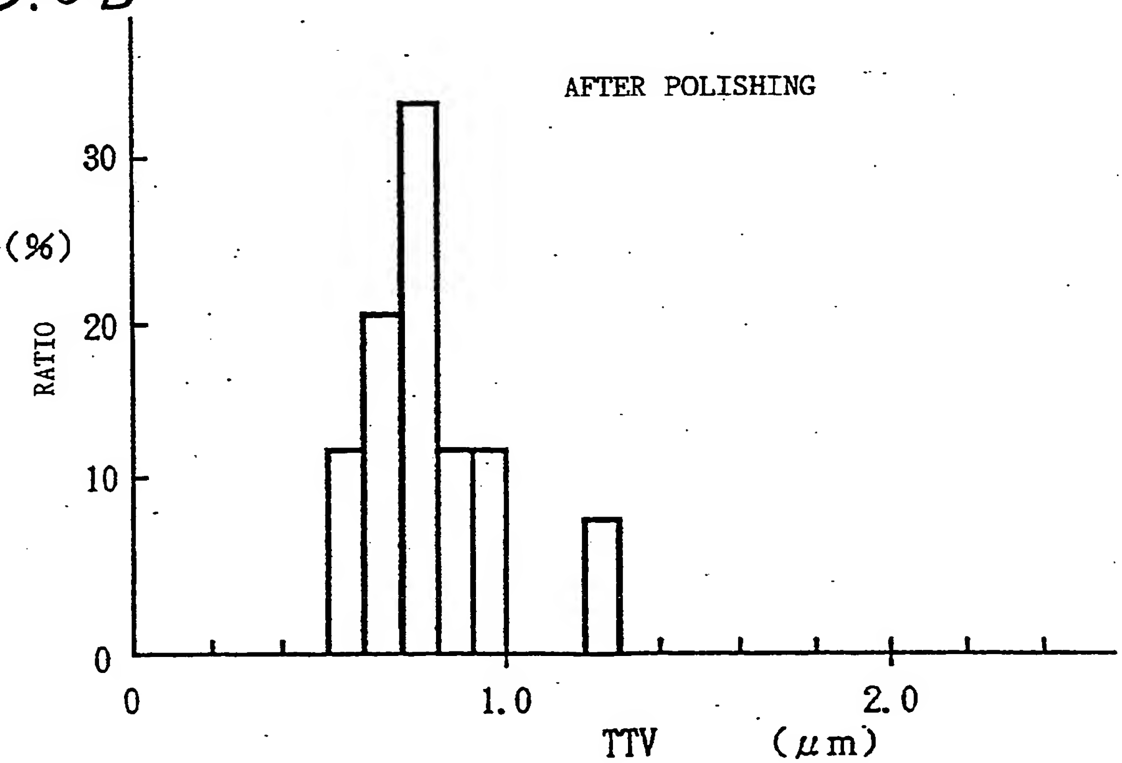

AFTER POLISHING
30
(%)
20
RATIO
10
0
0
1.0
2.0
TTV (μm)

FIG. 7A

WITHOUT OF

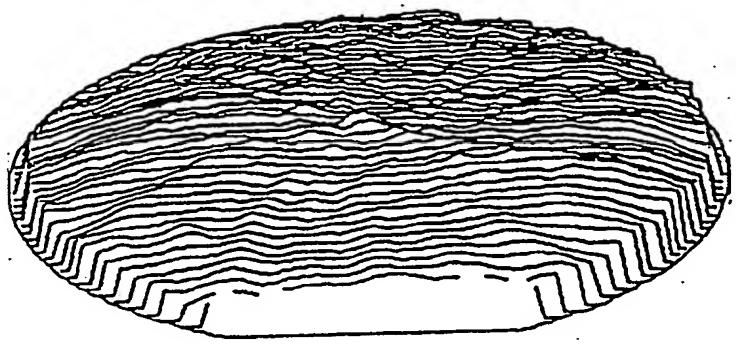


FIG. 7B

WITH OF

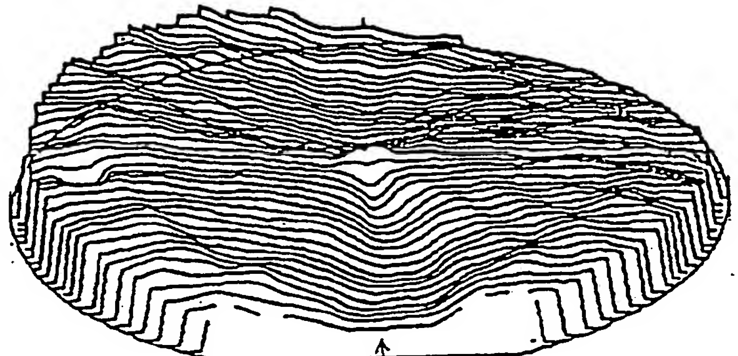


FIG. 8A

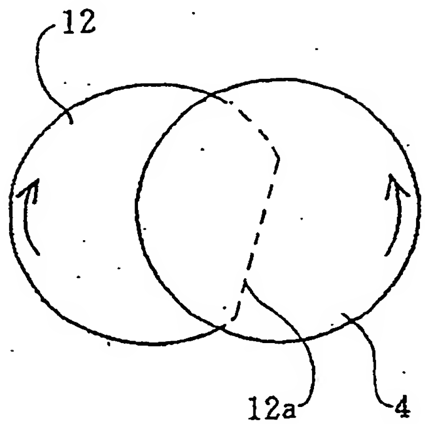


FIG. 8B

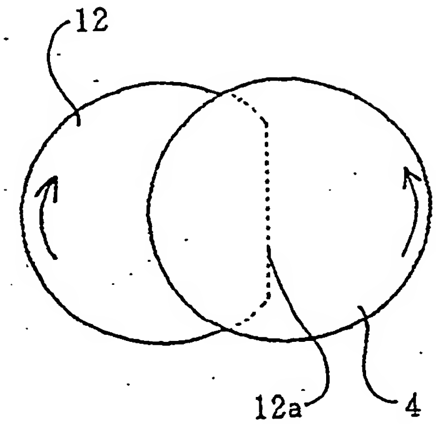


FIG. 8C

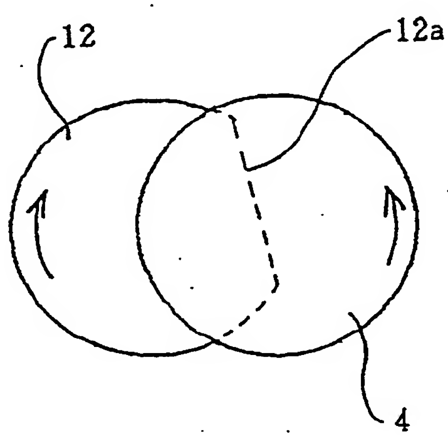


FIG. 8D

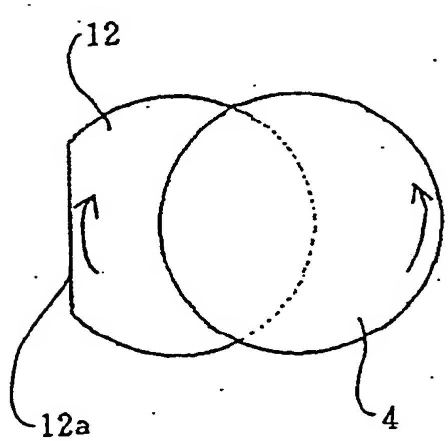


FIG. 9

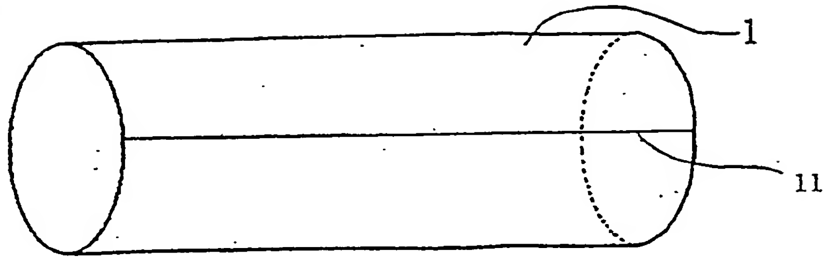


FIG. 10 A

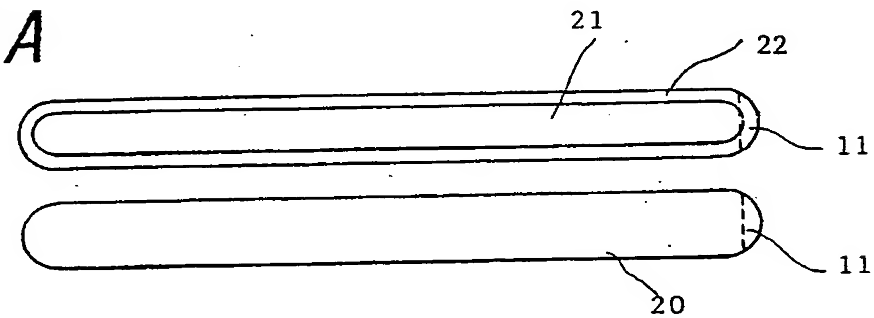


FIG. 10 B

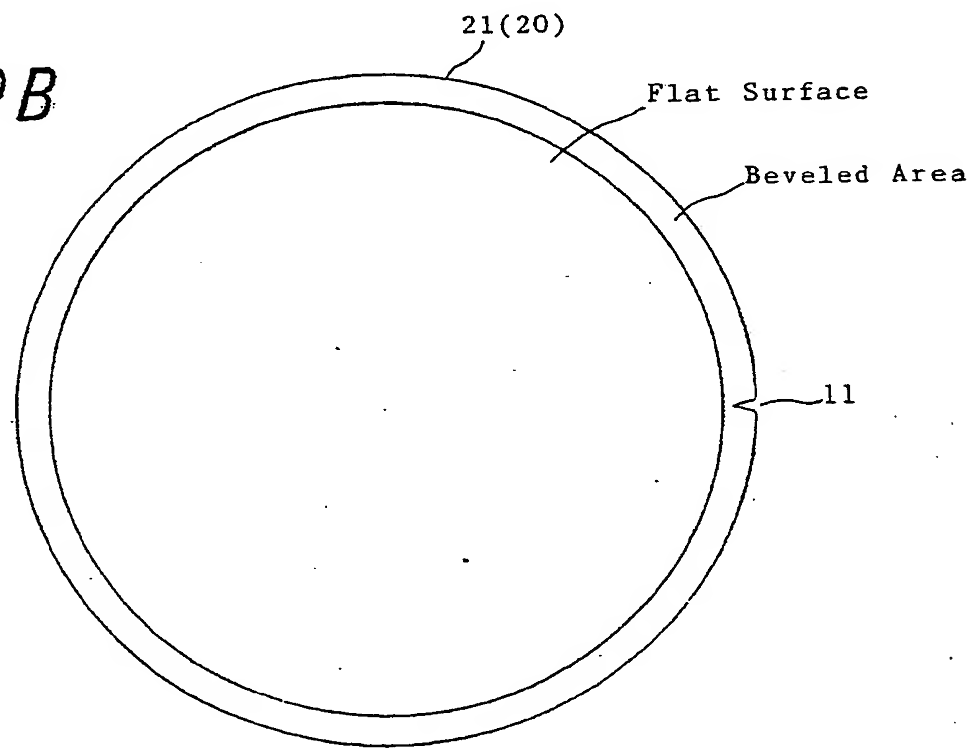


FIG. 10C

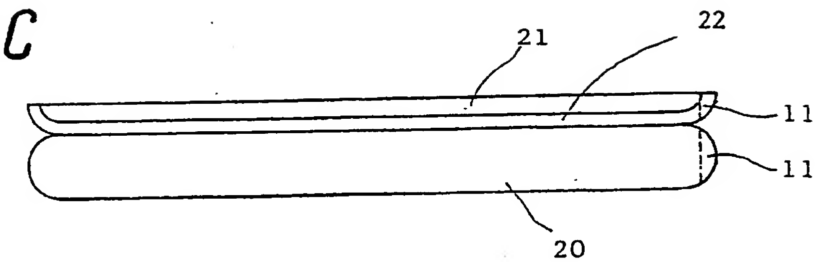


FIG. 10D

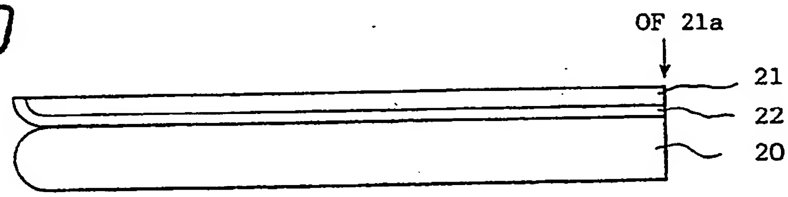


FIG. 10E

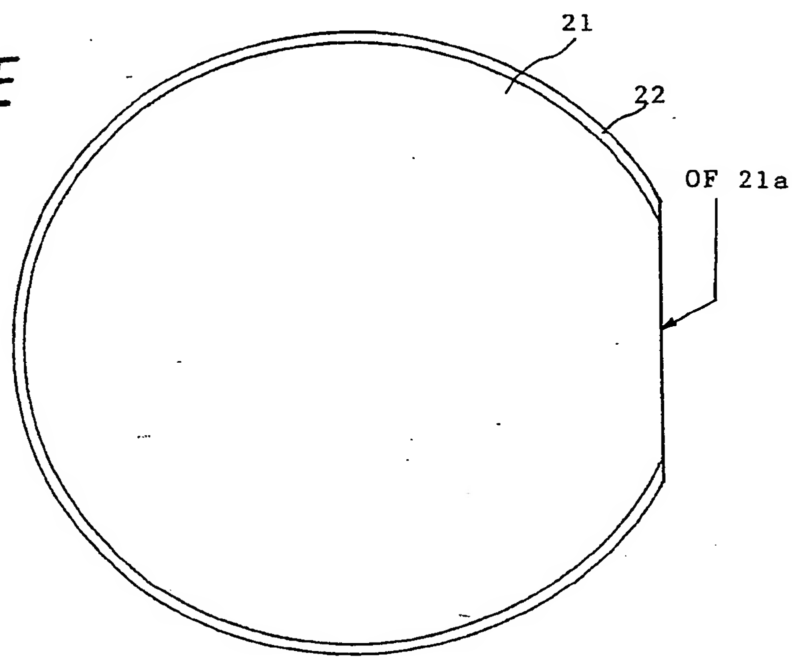


FIG. 11 A

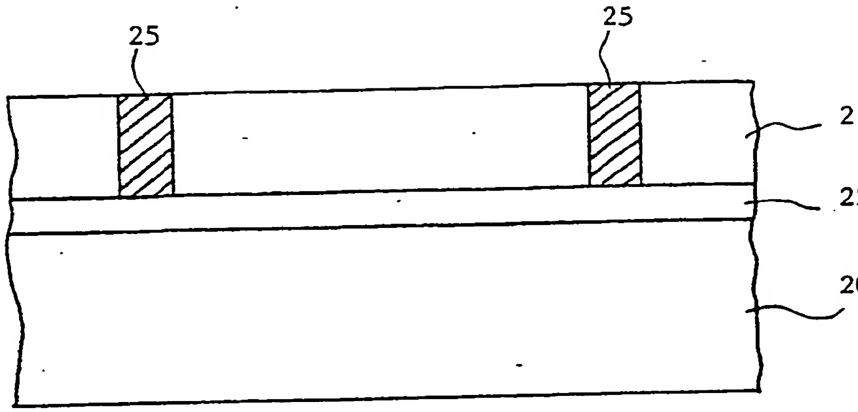


FIG. 11 B

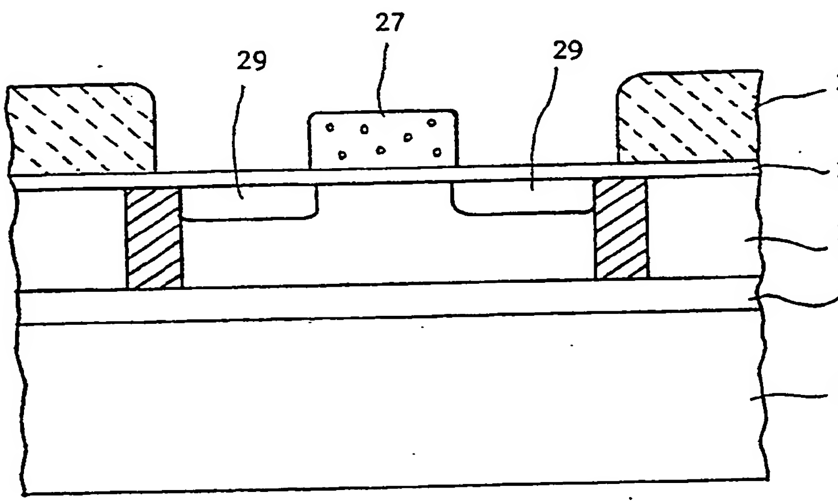
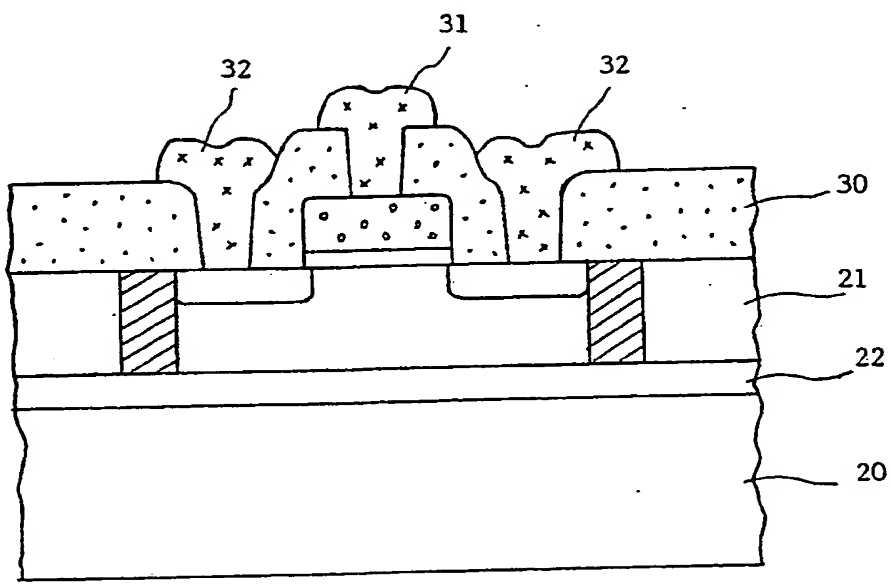


FIG. 11 C



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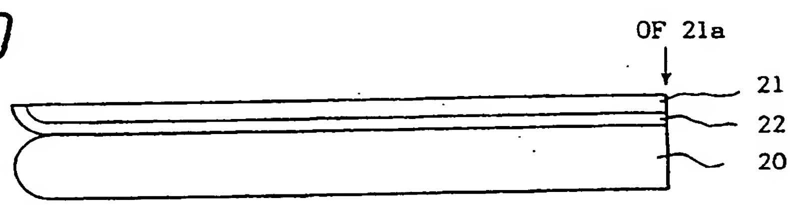
(54) **Method of manufacturing semiconductor substrate and method of manufacturing semiconductor device composed of the substrate.**

(57) Disclosed is a method of manufacturing a semiconductor wafer or SOI substrate having TTV of 1 micrometer or less which is required to make a future semiconductor integrated circuit of high density.
A semiconductor crystal disk (2; 12; 20, 21) made by slicing a semiconductor crystal ingot (1) is flattened by being subjected to a flattening step such as a grinding step (4), chemical-mechanical polishing or the like and then subjected to a step for providing an asymmetric configuration such as an orientation flat (OF) (12a, 21a) and the like. With this process, the deterioration of flatness due to the presence of the OF and the like can be prevented. Further, a flattening step conventionally carried out by a lapping step is replaced by surface grinding, by which the flatness of a wafer is improved and an etching step following to the lapping step can be omitted. The introduction of this process enables semiconductor wafers having a TTV of 1 micrometer or less and a diameter of 6 inches to be obtained at a yield of 90% or more. The application of the above method to an SOI substrate composed of two silicon wafers (20, 21) bonded through an insulating layer (22) can uniformly thin one of the silicon wafers to a few micrometers, whereby the practical use of a semiconductor integrated circuit of an SOI structure will be accelerated.

FIG. 10D



EP 0 460 437 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 91107952.3

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP - A - 0 319 805 (TOSHIBA) * Fig. 1,13; claim 1; column 3, lines 33-46 * --	1,8,9	H 01 L 21/304 H 01 L 21/76
A	EP - A - 0 226 772 (TOSHIBA) * Totality * --	1-3,7-9	
A	PATENT ABSTRACTS OF JAPAN, unexamined applications, M section, vol. 12, no. 27, January 27, 1988 THE PATENT OFFICE JAPANESE GOVERNMENT page 39 M 662; & JP-A-62 181 869 (SUMITOMO ELECTRIC IND. LTD.) --	1,2,8,9	
A	EP - A - 0 368 584 (SONY) * Fig. 1-4; column 4, line 23 - column 7, line 7 * --	1,2,8-12	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H 01 L B 24 B
P,A	EP - A - 0 418 737 (TOSHIBA) * Claims 1-9; abstract * ----	1-24	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	30-12-1994	HEINICH

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